Avionics Interface Technologies

APG-FC2/4
Hardware Manual

Dual Port Fibre Channel Simulator/Analyzer Interface
Test Module for PCI/PCI-X

September 2010

V03.00 Rev. A

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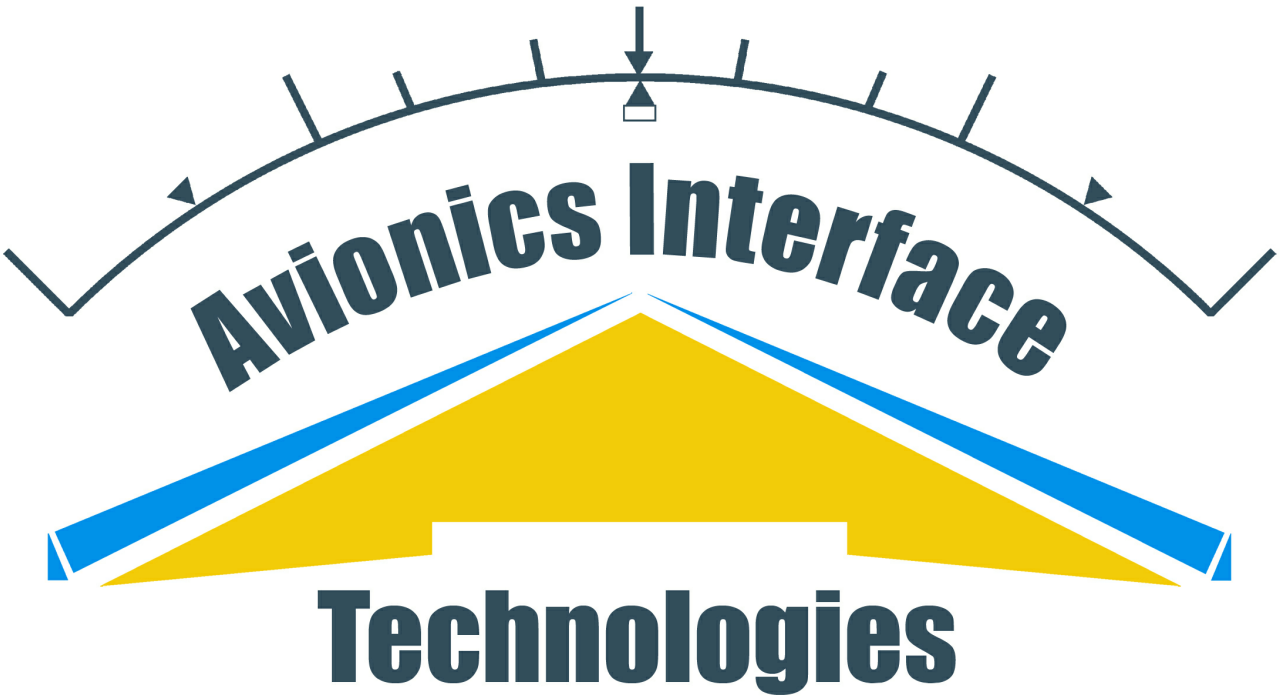

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> Product Overview
> MIL-STD-1553
> ARINC429
> Combination 1553/429
> ARINC664/AFDX
> MIL-STD-1760
> Fibre Channel
>> PCI/PCI-X
>> SDK
> TTEthernet
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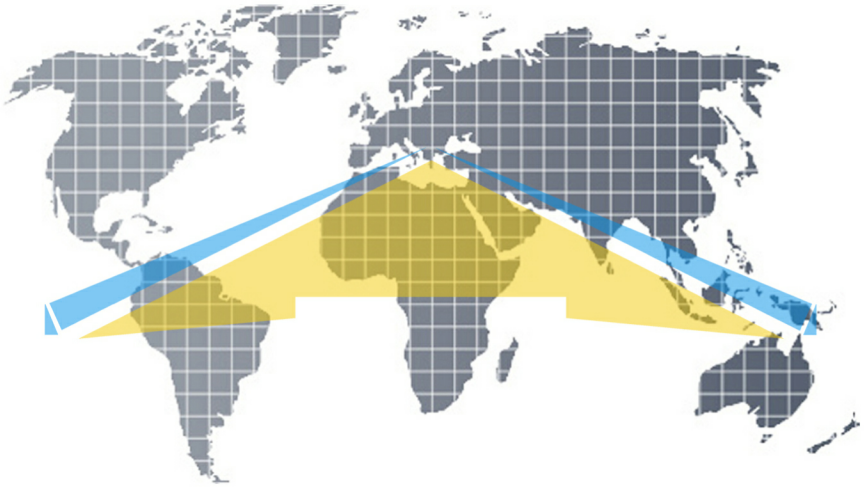

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Table of Contents

Section 1 INTRODUCTION 1

1.1 General 1

1.2 How This Manual is Organized 2

1.3 Applicable Documents 2

1.3.1 Industry Documents 2

1.3.2 Product Specific Documents 3

1.3.3 Fibre Channel Related Books 3

Section 2 STRUCTURE OF THE APG-FC4 4

2.1 FPGA 7

2.2 PowerPC RAM 8

2.3 Scalable Memory 8

2.4 Port Bypass 8

2.5 Time Sunchronization 8

2.6 Power Supply Circuitry 8

2.7 Transparent PCI Bridge 8

2.8 PCI Edge Connector 8

Section 3 EXTERNAL INTERFACES 9

3.1 Front Panel LEDs 9

3.2 SFP Fibre Channel Interface 10

3.3 I/O Interfaces for Timing and Triggers 10

Section 4 TIME SYNCHRONIZATION OPERATION (PRELIMINARY) 17

4.1 Time Synchronization Methods 17

4.2 Internal Board-to-Board Timer-Sync Connector and Switches 20

Section 5 BOARD LOGIC DESCRIPTION 23

5.1 IRIG Encoding/Decoding 23
5.2 PCI/PCI-X Interface 23
5.3 Port Logic 24
5.3.1 PowerPC 24
5.3.2 SERDES Interface 25
5.3.3 Analyzer 25
5.3.4 Generator 26
5.3.5 Media Access Controller (MAC) 26

Section 6 TECHNICAL DATA 27

Section 7 NOTES 30

7.1 Abbreviations and Acronyms 30

1 INTRODUCTION

1.1 General

This APG-FC4 Hardware Manual defines the board connections, a general description of the hardware architecture and technical data for the APG-FC4 *Simulyzer*™module for PCIbus and PCI-Xbus. For installation of the APG-FC4 and associated Software Development Kit (SDK), please see the **APG-FC4 Getting Started Manual**.

The APG-FC4 *Simulyzer*™ module is a member of AIT's family of high performance, intelligent Fibre Channel interface modules that offer full function testing, data generation/simulation and monitor/analyzer functions. The APG-FC4 modules have been developed to operate in-line or as a Node in Point-to-Point, Switched Fabric and Arbitrated Loop topologies. The APG-FC4 offers onboard processing, scalable memory resources, IRIG encoder/decoder and high speed protocol deciphering.

The advanced hardware architecture uses a Xilinx Virtex-II PRO which includes two Power PCs (PPC) (one for each Fibre Channel port). The dual ports function independently or can be configured to work together for a variety of specific modes of operation. A powerful PCIController and Memory Arbiter is realized in a Field Programmable Gate Array (FPGA). The FPGA supports the interface to the application, the software tasks running the host computer and assists the communication for data transfer. The IRIG encoder/decoder on the APG-FC4 board satisfies the requirements of 'multi-channel time tag synchronization' on a system level.

The APG-FC4 is available in one of the following options:

APG-FC4-xGB
- Dual Port Fibre Channel *Simulyzer*™, simultaneous Simulator and Analyzer for 4 Gbps data rates respectively.
- Memory: x = 1 GB, 2 GB, 4 GB RAM So-Dual Inline Memory Modules (DIMMs) (half per port)

APG-FC4-DC-xGB
- Dual Port Fibre Channel *Simulyzer*™ plus *Data Corruptor*™ for 4 Gbps data rates respectively.
- Memory: x = 1 GB, 2 GB, 4 GB RAM So-DIMMs (half per port)

APG-FC4-SF-xGB
- Dual Port Fibre Channel Single Function interface module, programmable to either Data Generator/Monitor or Analyzer for 4 Gbps data rates respectively.
- Memory: x = 1 GB, 2 GB, 4 GB RAM So-DIMMs (half per port)

DOCUMENT HISTORY

Version	Cover Date	Created by	Description
V1.00 Rev. B	January 2005	S. Lindsay	Creation of document
V1.00 Rev. C	March 2005	S. Lindsay	Apply new format
V2.00 Rev. A	August 2005	N. Kragick/ D. Dingeman	Added 4G information/ edited format
V3.00 Rev. A	September 2010	M. Amarawardana	Update technical specifications/apply new format

1.2 How This Manual is Organized

This hardware manual is comprised of the following sections:

Section 1, *INTRODUCTION*, contains an overview of this manual

Section 2, *STRUCTURE OF THE APG-FC4*, describes the main components, connector pinouts and logic functionality

Section 3, *EXTERNAL INTERFACES*, describes the faceplate I/O status and connectors including pin out description

Section 4, *TIME SYNCHRONIZATION OPERATION*, describes the methods and connectivity required to synchronize the timing for multiple APG-FC4 modules

Section 5, *BOARD LOGIC DESCRIPTION*, provides a high level overview of the board functionality and logic interfaces

Section 6, *TECHNICAL DATA*, provides technical specifications of the APG-FC4

Section 7, *NOTES*, Abbreviations and Acronyms

1.3 Applicable Documents

The following documents shall be considered to be a part of this document to the extent that they referenced herein. In the event of conflict between the documents referenced and the contents of this document, the contents of this document shall have precedence.

1.3.1 Industry Documents

The following American National Standards Institute (ANSI) Fibre Channel specifications were used to develop the APG-FC4 module design.

- FC Arbitrated Loop, ANSI X3.272:1996
- Fibre Channel Framing and Signaling Interface, ANSI/INCITS 373:2003

- Fibre Channel Framing and Signaling-2, T11/05-190v3 draft
- FC Generic Services, ANSI X3.288:1996
- Fibre Channel 2nd Generation Generic Services, ANSI NCITS 288
- Fibre Channel - Switch Fabric – 2, ANSI/NCITS 355-2001

1.3.2 Product Specific Documents

AIT has developed documents that may aid the user with other aspects of the APG-FC4 Fibre Channel module. These documents and a summary of their contents are listed below:

- **APG-FC4 Getting Started Manual**, assists the first time users of the AIT APG-FC4 boards and *fcXplorer* graphical user interface with software installation, hardware installation and starting a sample host application project
- **APG-FC4 Software Library Reference Manual for Windows and Linux Applications**, provides the user with detailed APG-FC4programming information including Application Interface function calls, header file details and Sample Program descriptions
- ***fcXplorer* User's Manual**, provides definition and step-by-step instructions on how to use *fcXplorer*, the Fibre Channel Simulator and Analyzer Test Software for Windows, *fcXplorer* provides a Graphical User Interface to setup and control the APG-FC4

1.3.3 Fibre Channel Related Books

- Fibre Channel; A Comprehensive Introduction, Robert W. Kembel, Northwest Learning Associates, 3061 N. Willow Creek Drive, Tucson, AZ 85712. See www.nlabooks.com.
- The Fibre Channel Consultant: Arbitrated Loop, Robert W. Kembel, Northwest Learning Associates, 3061 N. Willow Creek Drive, Tucson, AZ 85712. See www.nlabooks.com.
- The Fibre Channel Consultant: Fibre Channel Switched Fabric, Robert W. Kembel, Northwest Learning Associates, 3061 N. Willow Creek Drive, Tucson, AZ 85712. See www.nlabooks.com.

2 STRUCTURE OF THE APG-FC4

The APG-FC4 module architecture consists of the following main components as described in the following sections:

- Field Programmable Gate Array (FPGA)
- Power PC RAM
- Scalable Memory
- Port Bypass
- Time Synchronization
- Power Supply Circuitry
- Transparent PCI Bridge
- PCI Edge Connector

Figures 2-1 and 2-2 provide an overview of the hardware architecture for the APG-FC4 DSUB and MOD8 configurations respectively.

Figures 2-3 and 2-4 show the main components of the APG-FC4 DSUB and MOD8 configurations respectively.

Figure 2-1 APG-FC4 Hardware Architecture (DSUB Configuration)

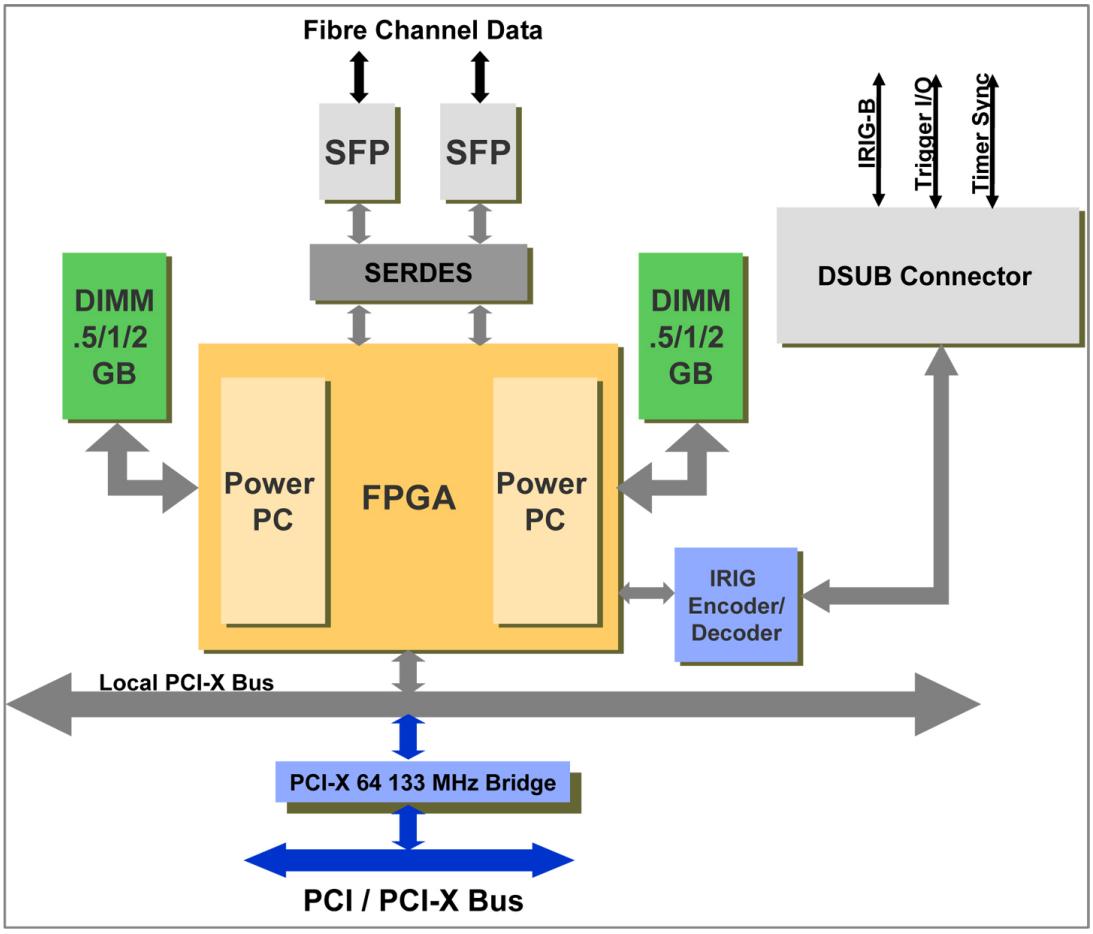


Figure 2-2 APG-FC4 Hardware Architecture (MOD8 Configuration)

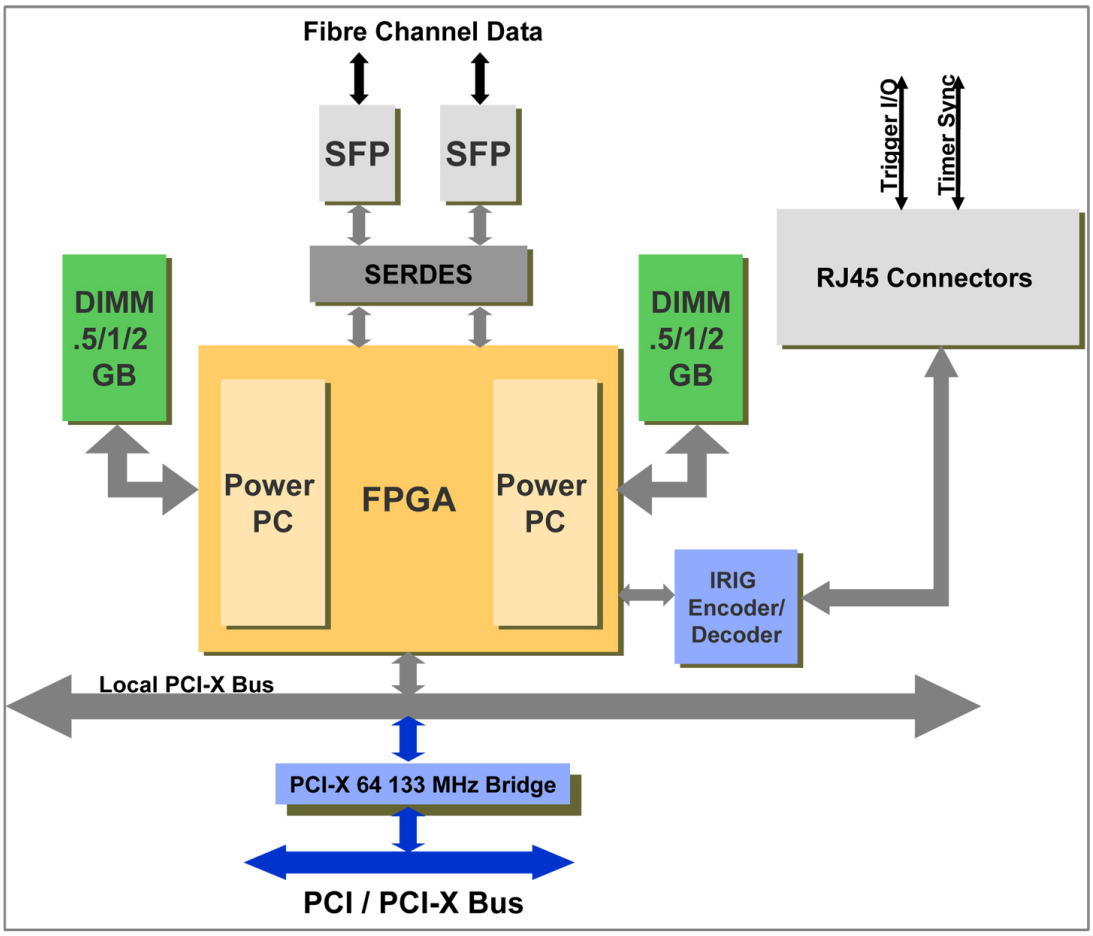


Figure 2-3 APG-FC4 Board Hardware Overview (DSUB Configuration)

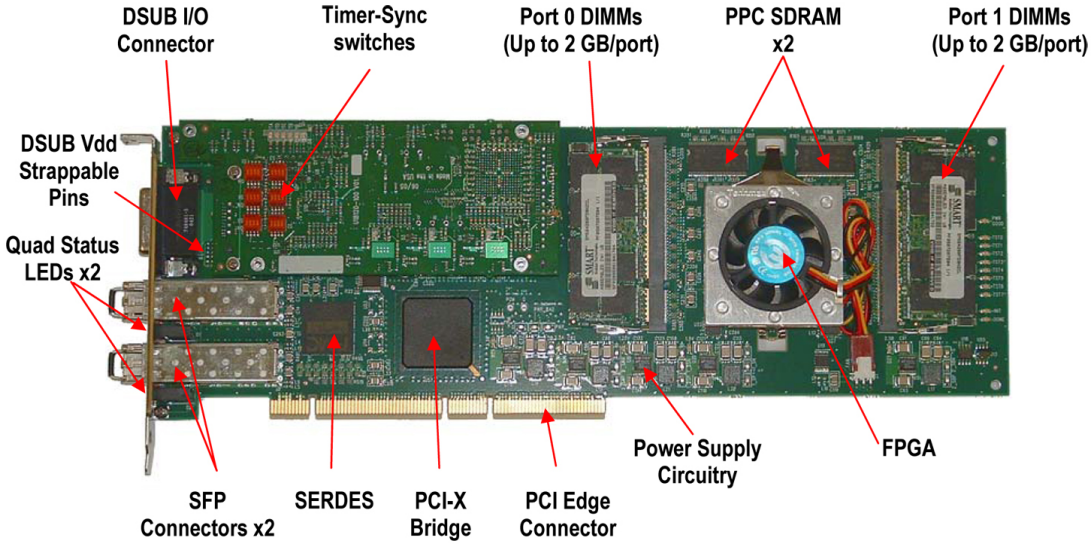
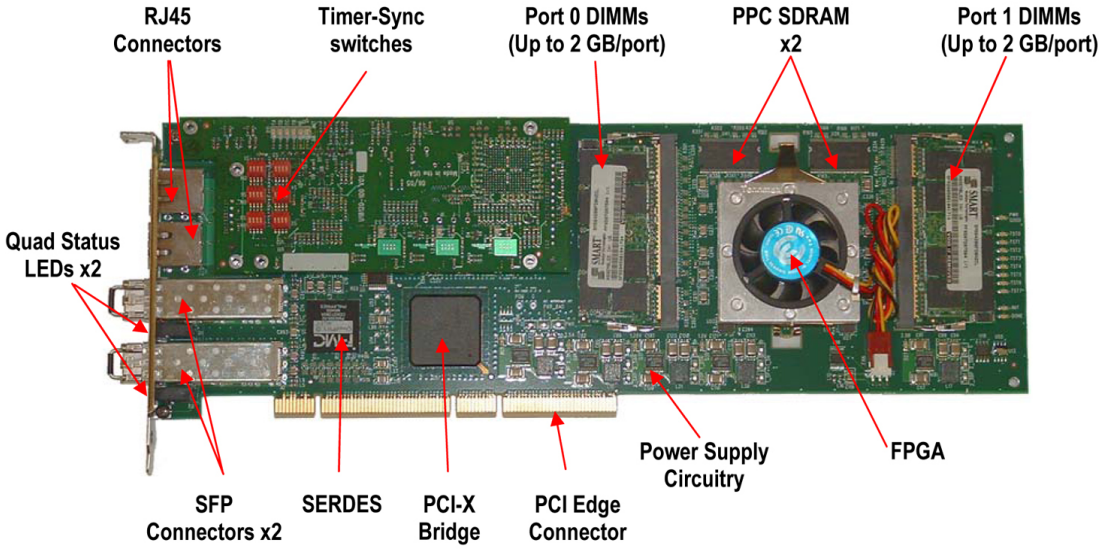


Figure 2-4 APG-FC4 Board Hardware Overview (MOD8 Configuration)



2.1 FPGA

The FPGA on the APG-FC4 contains the port logic for both Fibre Channel ports and glue logic for connecting together the board components. Each port is equipped with a 32-bit PowerPC processor for running customer applications and some of the Fibre Channel port logic (loop initialization, etc.)

2.2 PowerPC RAM

Each port on the APG-FC4 has dedicated memory for its PowerPC processor. This memory stores the data, instruction, heap and stack segments for user programs and the application interface.

2.3 Scalable Memory

The APG-FC4 can be configured with 512MB, 1 GB, or 2 GB of RAM per port. The APG-FC4 can additionally be configured with 4 GB of RAM per port. This RAM is used for user transmit data and monitor data.

2.4 Port Bypass

The APG-FC4 provides an external bypass for incoming data, so that data coming in one port may be repeated out the second port without passing through the FPGA. This provides the lowest possible latency from the input to the output on the card while maintaining signal integrity. Both cards will wrap the data internally as well, which increases latency but improves the transmitted signal quality.

2.5 Time Sunchronization

Both an IRIG encoder and decoder are included on the APG-FC4 card. This circuitry is used to synchronize multiple APG-FC4 cards together in the system, and to synchronize timestamps with other IRIG-B cards in a larger system. On the APG-FC4, this time synchronization circuitry is part of a daughter card. See Section 4 for more information regarding configuration of timing interfaces for multiple APG-FC4 boards.

2.6 Power Supply Circuitry

Power is supplied from the +5V and +12V rails of the PCI edge connector. All other required voltages are generated on the board using DC-DC Converters.

2.7 Transparent PCI Bridge

The transparent PCI bridge isolates the FPGA from the system PCI bus or PCI-X bus. This allows the APG-FC4 to operate in both + 5V and +3.3V PCI signaling environments.

2.8 PCI Edge Connector

The PCI edge connector is keyed for both +3.3V an +5.0V signaling environments. On the APG-FC4, this interface is strapped to identify the card as a 133 MHz 64-bit PCI-X device.

3 EXTERNAL INTERFACES

The APG-FC4 faceplate provides external interfaces for the following:

- Status LEDs
- SFP Fibre Channel interface
- I/O Interface for triggers and IRIG-B
- Timing interface for synchronization of multiple boards (APG-FC4 only)

Figures 3-1 and 3-2 show the APG-FC4 DSUB and MOD8 faceplate configurations respectively.

3.1 Front Panel LEDs

Each port has four status LEDs located on the faceplate adjacent to its corresponding SFP socket, port 0 and port 1. Table 3.1-I describes the LEDs.

Table 3.1-1 LED Descriptions

LED Name	Color	Description
SIGNAL DETECTED	Yellow	Indicates the port is detecting light on the Fibre Channel interface
LINK ACTIVE	Yellow	Indicates success of the initialization of the port sequence for either Point-to-Point (N_Port) or Arbitrated Loop Topology (L_Port)
Tx/Rx FRAME	Yellow	Indicates the port is transmitting or receiving frames
LINK ERROR	Red	Indicates the port has detected FC1 or FC2 errors on the receiver

Figure 3.1-1 APG-FC4 DSUB Faceplate

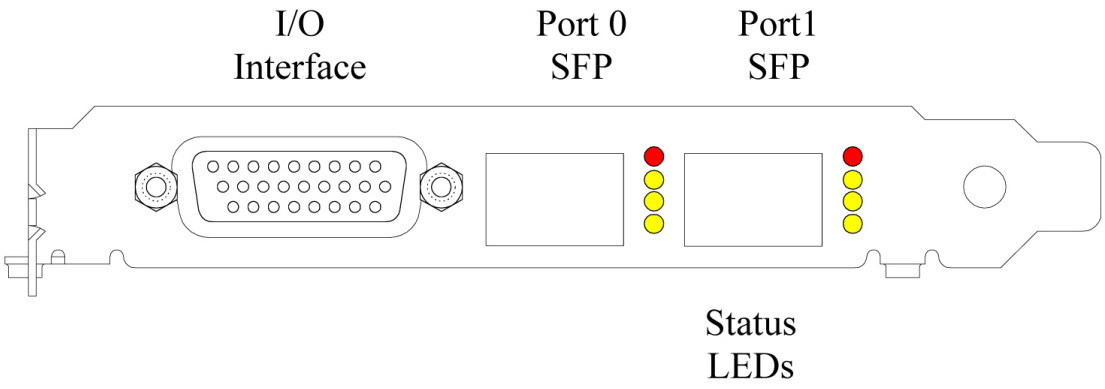
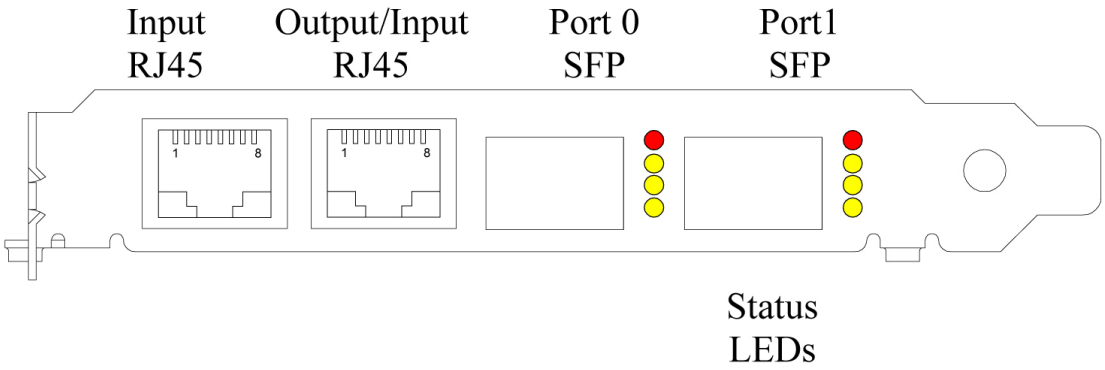


Figure 3.1-2 APG-FC4 MOD8 Faceplate



3.2 SFP Fibre Channel Interface

The APG-FC4 module utilizes two Small Form-factor Pluggable (SFP) sockets (port 1 and port 2) located on the front panel. These sockets accept either wire (copper) or fiber transceivers. The AIT-provided optical transceivers employ modular LC™ connectors and are powered by a single 3.3 V power source supplied by the board. The wire transceivers are available in a variety of connectors.

3.3 I/O Interfaces for Timing and Triggers

Each APG-FC4 board contains an I/O connector (DSUB-26 pin connector or an RJ45 connector) on the faceplate for timing and trigger interfaces. This section describes the timing and I/O interface for each board type.

The APG-FC4 is available in two configurations that support different I/O connections as follows:

- **APG-FC4 with High Density DSUB-26 pin female connector** - All IRIG, timer

sync, and trigger inputs/outputs are routed through this connector. The connector pin outs are shown in Figure 3.3-2.

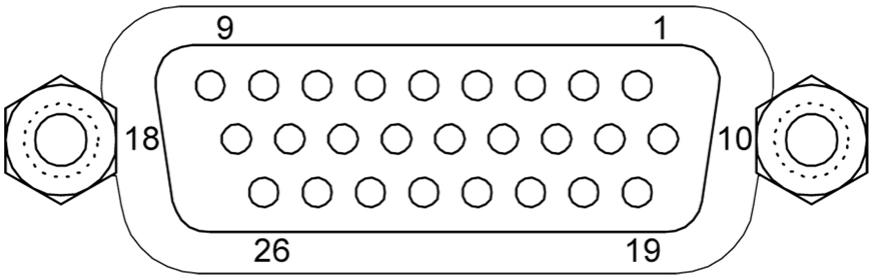
- **APG-FC4 with two 8-pin RJ45 female connectors** - Only sync and trigger inputs/outputs are routed through these connectors. (IRIG is not available using these connectors.) The connector pin outs and RJ45 signal I/O schematic are shown in Figure 3.3-3.

These connectors use standard CAT5 UTP (EIA/TIA-568A) cables for timing interconnections. Shielded cables can also be used to keep magnetic radiation to a minimum. To keep timing skew to a minimum, use as short a cable as is practical.

Note: Trigger outputs will also be connected to the next modules trigger inputs and will not be daisy chained, even when switches are in daisy chain position.

Switches on the I/O connector circuit board determine if the second connector (Connector B) is an output connector or is wired in parallel with the input connector for daisy chaining the sync signals. (trigger outputs are still outputs and are not changed by the switch.)
The first module in the chain (usually master) must be set to 'Output'. All other modules can be set to 'Daisy' (up to 15 modules). If more than 15 are chained, number 15 should be set to 'Output' to buffer the signals for the next modules. See Section 4 for further information regarding synchronization of timing.

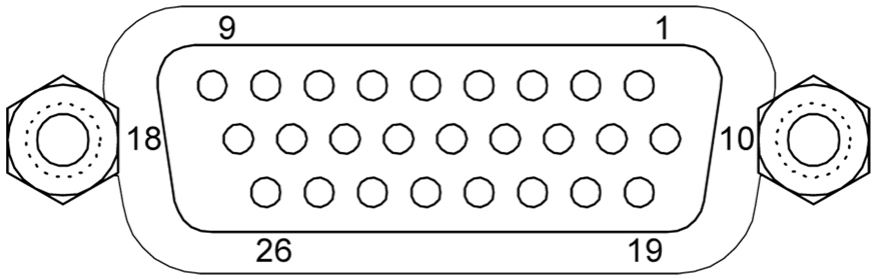
Figure 3.3-1 APG-FC2 External I/O Interface



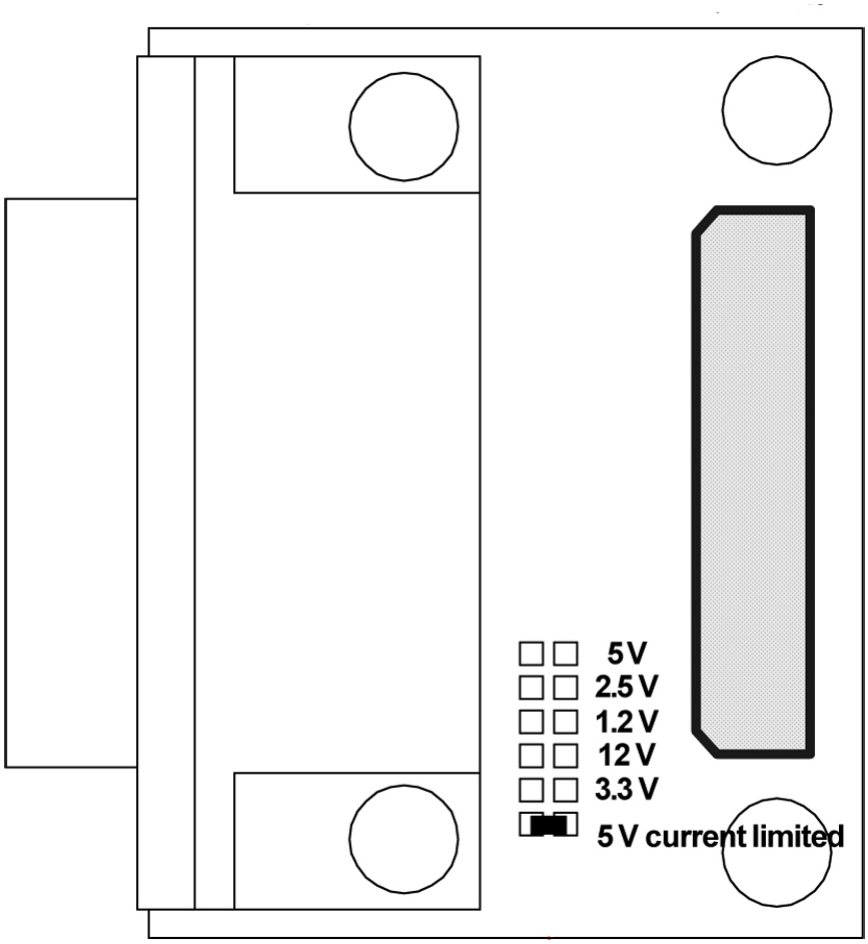
Looking into panel DSUB connector

Pin No.	Signal
1	NO CONNECT
2	NO CONNECT
3	NO CONNECT
4	TRIG1_IN GND
5	TRIG1_IN
6	NO CONNECT
7	NO CONNECT
8	+12 VDC GND
9	NO CONNECT
10	+12 VOLTS
11	NO CONNECT
12	NO CONNECT
13	TRIG0_IN
14	TRIG0_IN GND
15	TRIG1_OUT
16	TRIG1_OUT GND
17	IRIG_IN
18	IRIG_IN GND
19	NO CONNECT
20	NO CONNECT
21	TRIG0_OUT GND
22	TRIG0_OUT
23	NO CONNECT
24	NO CONNECT
25	IRIG_OUT GND
26	IRIG_OUT

Figure 3.3-2 APG-FC4 with DSUB 26-pin External I/O Interface



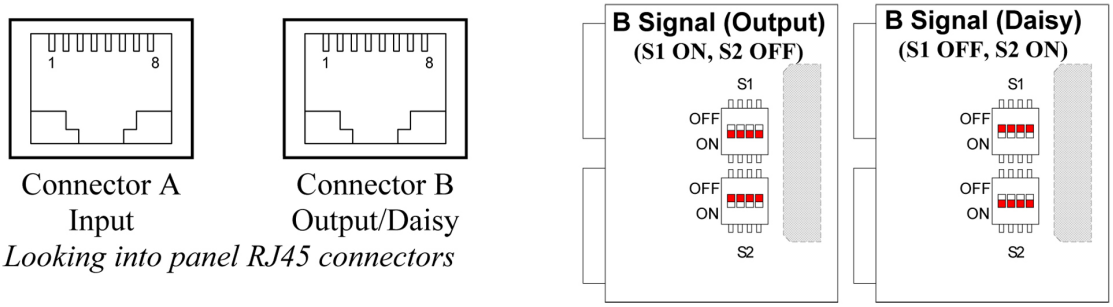
Looking into panel DSUB connector



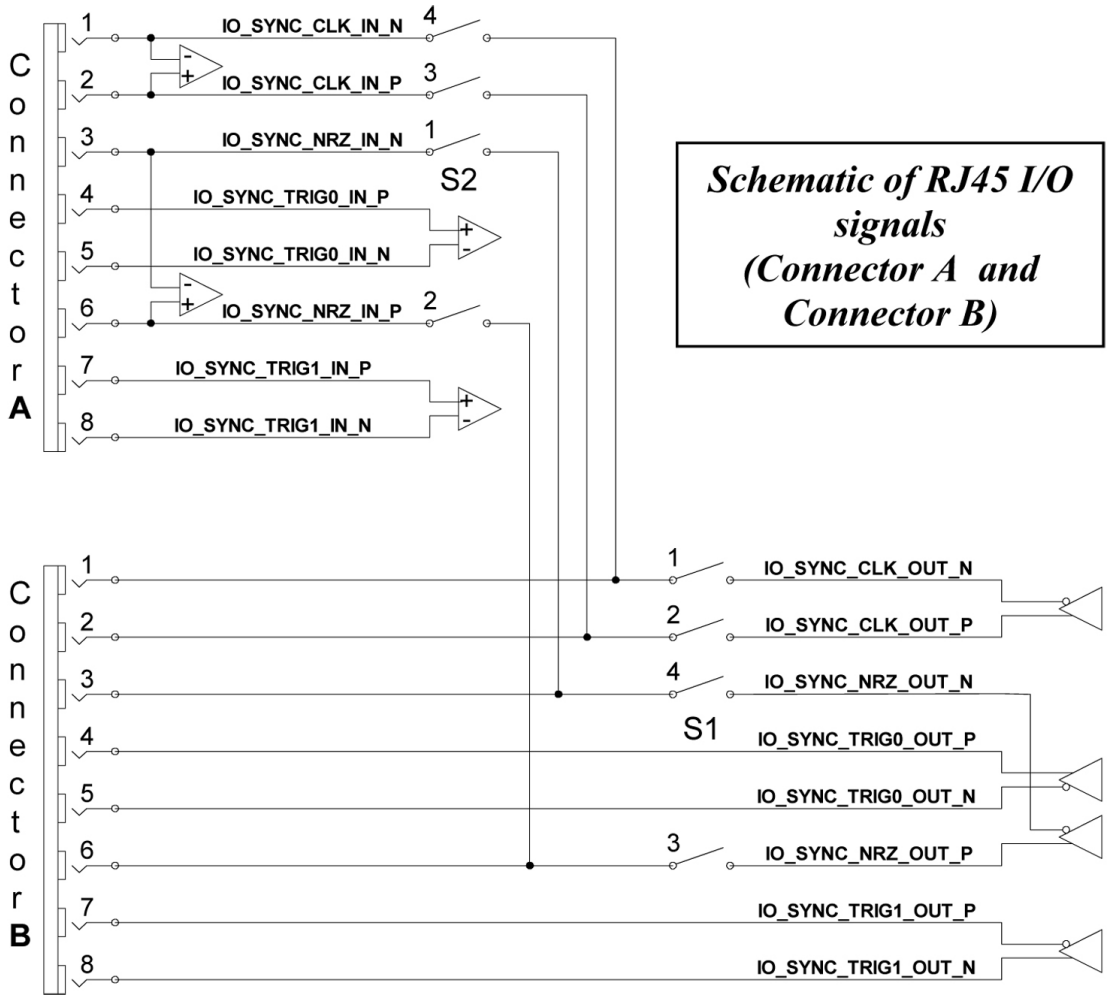
Looking above DSUB connector

Pin No.	Signal
1	SYNC_CLK_OUT_N
2	SYNC_CLK_OUT_P
3	SYNC_NRZ_IN_P
4	SYNC_NRZ_IN_N
5	TRIG1_IN_P
6	TRIG1_IN_N
7	SYNC NRZ_OUT_P
8	SYNC NRZ_OUT_N
9	NO CONNECT
10	Vdd (strappable - factory default 5.0 volts) for auxiliary use only (normally unused)
11	GND
12	GND
13	TRIG0_IN_P
14	TRIG0_IN_N
15	TRIG1_OUT_P
16	TRIG1_OUT_N
17	IRIG_IN_P
18	IRIG_IN_N
19	SYNC_CLK_IN_N
20	SYNC_CLK_IN_P
21	TRIG0_OUT_N
22	TRIG0_OUT_P
23	SYNC_PULSE_IN_N
24	SYNC_PULSE_IN_P
25	IRIG_OUT_N
26	IRIG_OUT_P

Figure 3.3-3 APG-FC4 with RJ45 External I/O Interface



Pin No.	A Signal (Input)	B Signal (Output)	B Signal (Daisy)
		(S1 ON S2 OFF)	(S1 OFF S1 ON)
1	SYNC_CLK_IN_N	SYNC_CLK_OUT_N	SYNC_CLK_IN_N
2	SYNC_CLK_IN_P	SYNC_CLK_OUT_P	SYNC_CLK_IN_P
3	SYNC_NRZ__IN_N	SYNC_NRZ_OUT_N	SYNC_NRZ_IN_N
4	TRIG0_IN_P	TRIG0_OUT_P	TRIG0_OUT_P
5	TRIG0_IN_N	TRIG0_OUT_N	TRIG0_OUT_N
6	SYNC_NRZ_IN_P	SYNC_NRZ_OUT_P	SYNC_NRZ_IN_P
7	TRIG1_IN_N	TRIG1_OUT_N	TRIG1_OUT_N
8	TRIG1_IN_P	TRIG1_OUT_P	TRIG1_OUT_P



Schematic of RJ45 I/O signals (Connector A and Connector B)

4 TIME SYNCHRONIZATION OPERATION (PRELIMINARY)

When multiple APG-FC4 boards are contained in a system, synchronization of the timing signal is important when comparison of capture logs is required and/or synchronization of module processes are required.

The time stamps saved in the capture log are derived from a set of counters running inside the FPGA. Two counters are used, a Most Significant Bits (MSB) counter and a Least Significant Bits (LSB) counter. The MSB counter holds the day/hour/minute/seconds and is loaded by the IRIG decoder or manually by the user. The Least Significant Bits (LSB) counter holds fractions of seconds.

Synchronization of the timing counters will occur every second except while the Chronological monitor is actively capturing data. Synchronization will cause the LSB counter to be reset to 0 by the sync signal (either the external IRIG signal or timer sync signal), or by a manual load. The time stamp format is shown in Table 4-I

Table 4-1 Time Elements and Bits

Time Element	Number of digits
DAYS of Year	3
HOURS of Day	2
MINUTES of Hour	2
SECONDS of Minute	2
NANOSECONDS of Second (10 μs)	5

4.1 Time Synchronization Methods

The APG-FC4 provides two methods for synchronizing the time for multiple boards in a system as follows:

- **IRIG-Modulated Square Wave** - the IRIG modulated square wave generated by the logic in the FPGA on the master module can be used as input to each of the other IRIG inputs on the slave modules. An external IRIG-B signal, the host system clock or user-provided time can be used as the time source for the master module.

When an IRIG input signal is present, a 100 MHz IRIG PLL will be locked to the IRIG carrier. Time delay from connector, through the IRIG circuitry and to the time registers is nominally 170 ns with signal level of 0.2 to 2 volts p-p and then rises to 280 ns at 10 volts p-p. If the IRIG signal is a sine wave, the slow rise time will result in additional time skew (usually more delay due to hysteresis in comparators). Noise on the signal will result in increased timing jitter that is exacerbated by the slow rise time of a sine wave through the comparator threshold. The higher the signal level a sine wave has, the faster the rise time is and the better the signal to noise ratio. So it is best to use a level

of 2 to 3 volts pp if available. For this reason, the IRIG output from the modules is an amplitude modulated square wave instead of a sine wave. The fast rise and fall times virtually eliminate this component of skew and minimize impact of noise. Using daisy chaining from the master to the slaves on the square wave IRIG time-sync signal will result in the master being approximately 170 ns ahead of the slaves, and the slaves should be within 20 ns of each other. The units are phase locked to each other and the IRIG source, so skew is the only source of timing error in addition to the inaccuracy of the IRIG source. When no IRIG signal is present, or the module is set for internal timing, the IRIG PLL is configured to free run at 100 MHz with a 100 ppm tolerance.

- **SYNC_CLK and SYNC_NRZ signals** - the SYNC_CLK and SYNC_NRZ signals generated by the logic in the FPGA on the master module can be used as inputs to each of the other SYNC_CLK and SYNC_NRZ signal inputs on slave modules.

  This is the preferred method of synchronization for all APG-FC4 installations.

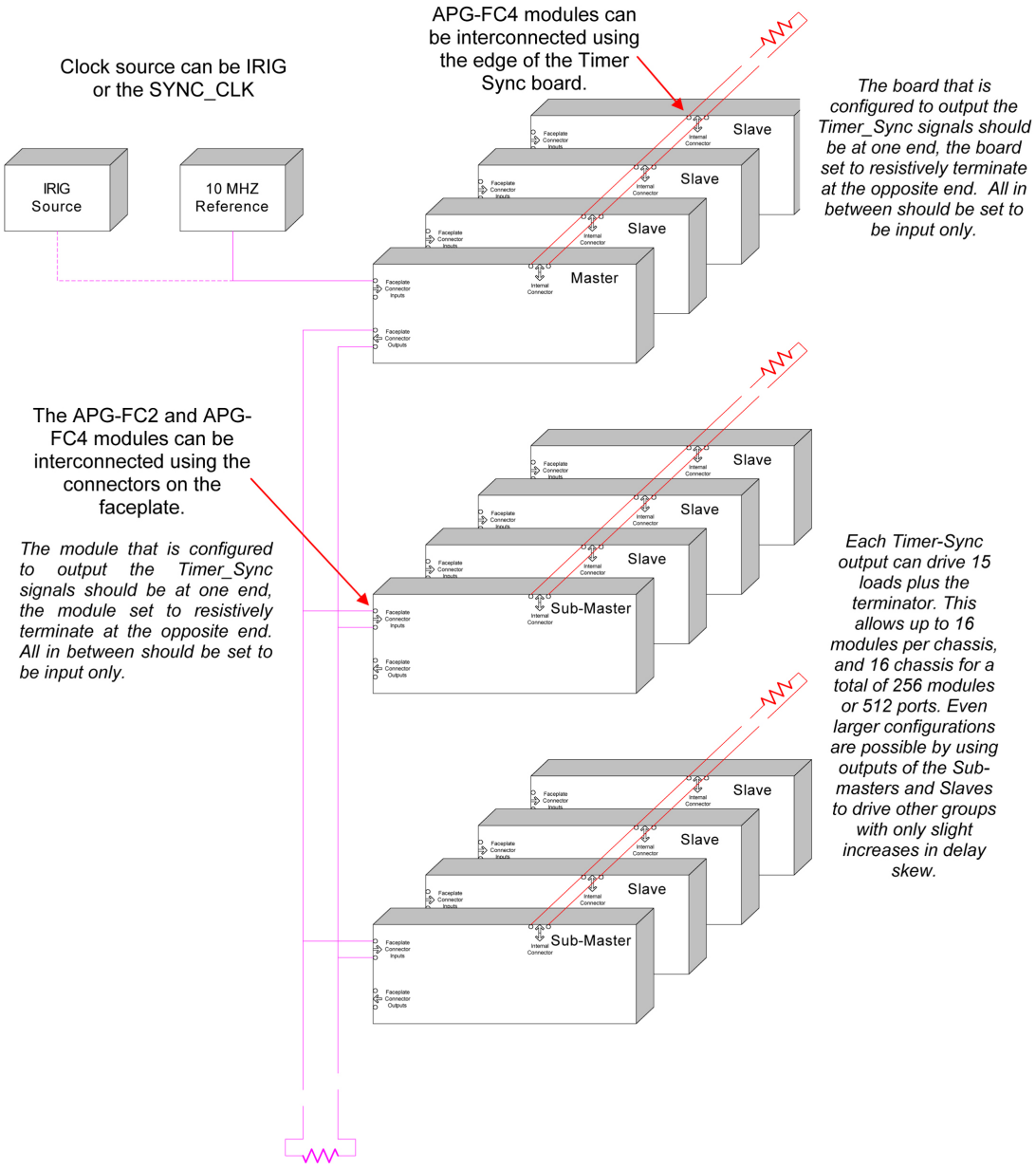
- **SYNC_CLK -** 10 MHz square wave 3ns (tentative) skew from clock source, rising edge is time sync aligned, falling edge is clock for SYNC_NRZ. (used for nanoseconds resolution.)
- **SYNC_NRZ -** 10 Mbps NRZ signal containing the MSB counter (used for seconds resolution)

The interconnection of multiple modules is implemented using the DSUB or RJ45 connector on the faceplate (as described in Section 3.3) or the connector on the top edge of the Timer-Sync board (for internal connection only on APG-FC4) (or both connection methods in the case of multiple groups of modules). Figure 4.1-1 provides an example of multiple groups of APG-FC4 modules connected to one external time source (either IRIG-B or SYNC_CLK). One module in the system is set up as a master and the rest are set up as slaves or as sub masters. (Table 4.1-I provides a description of the APG-FC4 module hierarchy terminology used in the timing synchronization example.)

Table 4.1-1 Timing Synchronization Example Terminology

Module Hierarchy	Description
Master Module	A module configured and wired to take a time reference such as an IRIG input or external or internal quartz referenced clock and generate the time sync signal(s). Normally a system would have a single Master Module.
Sub-Master Module	A module configured and wired to buffer time sync signals for use by itself and Slave. There is actually no configuration difference between a Sub-Master and a Slave module. The only difference is the way the time sync signals are connected to it. The time sync outputs of a Sub-Master are used as inputs by other modules. (The only reason a sub-master is here defined is for sake of verbal discussions about the interconnection of groups of modules).
Slave Module	A module configured and wired to buffer time sync signals for use only by itself is referred to as a Slave Module. There is actually no configuration difference between a Sub-Master and a Slave module. The only difference is the way the time sync signals are connected to it. The time sync outputs are not wired to anything with a slave.

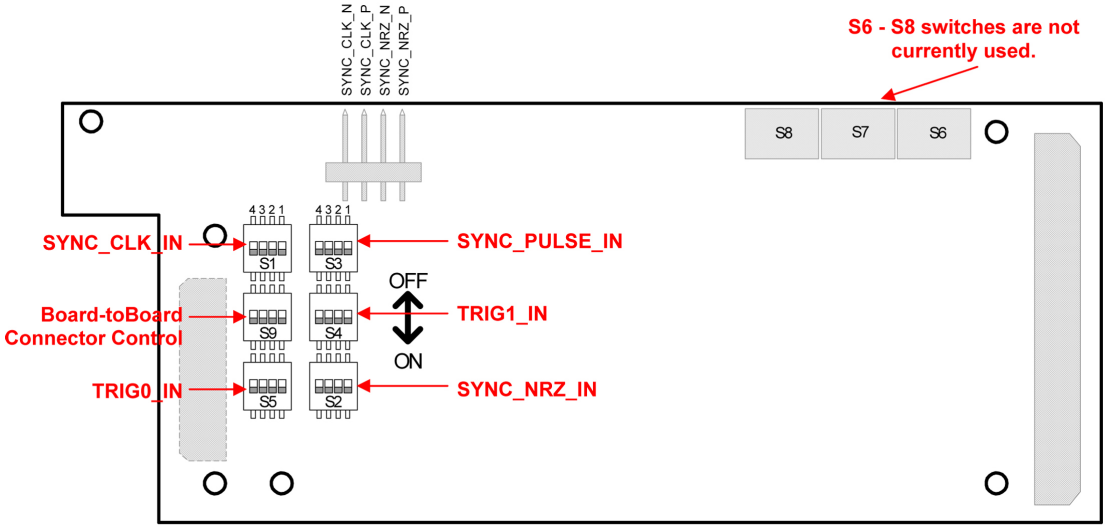
Figure 4.1-1 Timing Synchronization Interconnection Example


APG-FC4 modules can be interconnected using the edge of the Timer Sync board.
Clock source can be IRIG or the SYNC_CLK
IRIG Source
10 MHZ Reference
Slave
Slave
Slave
Master
The board that is configured to output the Timer_Sync signals should be at one end, the board set to resistively terminate at the opposite end. All in between should be set to be input only.
The APG-FC2 and APG-FC4 modules can be interconnected using the connectors on the faceplate.
The module that is configured to output the Timer_Sync signals should be at one end, the module set to resistively terminate at the opposite end. All in between should be set to be input only.
Slave
Slave
Slave
Sub-Master
Each Timer-Sync output can drive 15 loads plus the terminator. This allows up to 16 modules per chassis, and 16 chassis for a total of 256 modules or 512 ports. Even larger configurations are possible by using outputs of the Sub-masters and Slaves to drive other groups with only slight increases in delay skew.
Slave
Slave
Slave
Sub-Master

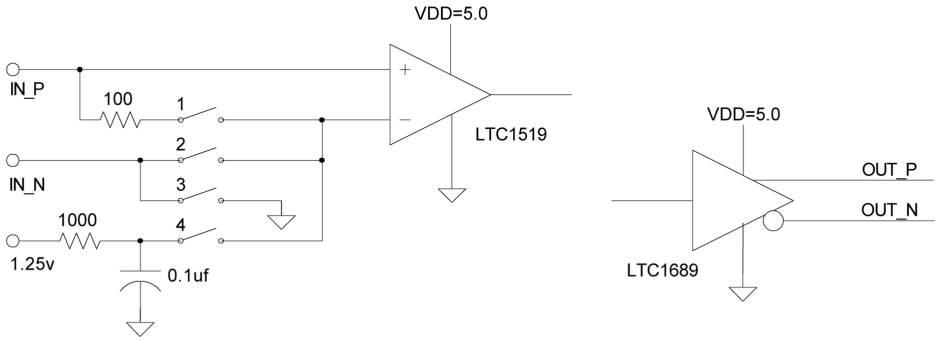
4.2 Internal Board-to-Board Timer-Sync Connector and Switches

APG-FC4 modules can be interconnected using the edge of the Timer Sync board. When using this method to interconnect your modules you must configure the six board to board Timer-Sync switches. These switches and associated input/output schematic are shown in Figure 4.2-1. Each switch contains 4 sub-switches (S*x*-1 through S*x*-4). The definition of each sub-switch for S1 – S5 is contained in Table 4.2-1. The definition for each sub-switch for S9 is contained in Table 4.2-2.

Figure 4.2-1 Board-to-Board Timer-Sync Switches and Schematic



Note: On the back of the Timer Sync board, the trimmer R45 adjusts the TCXO precision (not shown on diagram above). DO NOT adjust.



Schematic of logic inputs and outputs for S1 through S5.

Table 4.2-1 Timer-Sync Sub-Switches (Sx-1 through Sx-4) Definition for Switches S1 through S5

Name	Type	Threshold	Apply to IN_P	Apply to IN_N	Sx-1	Sx-2	Sx-3	Sx-4
RS485 unterminated	Differential		Positive Signal	Negative Signal	Off	On	Off	Off
RS485 terminated	Differential		Positive Signal	Negative Signal	On	On	Off	Off
CMOS	Single Ended	1.25 volt threshold	Positive Signal	Signal Return (GND)	Off	Off	On	On
CMOS Custom	Single Ended	Desired threshold (-7 to +12 limit)	Positive Signal	Threshold Voltage	Off	Off	On	On

*x = 1-5 (Other possibilities exist, see schematic and data sheets for devices.)

Note: Use RS485 unterminated except at the end of the line when interconnecting modules - where it will be terminated.

Table 4.2-2 Timer-Sync Sub-Switches (Sx-1 through Sx-4) Definition for Switch S9

S9 Sub-Switch	**Definition**
S9-1	Not used
S9-2	On to enable output driver on board-to-board connector (Master or Sub-Master)
S9-3	On to terminate SYNC_CLK with 100 ohms on board-to-board connector (end of line opposite Master)
S9-4	On to terminate SYNC_NRZ with 100 ohms on board-to-board connector (end of line opposite Master)

S9 Sub-Switch Setting	**Master**	**Slave**	**Terminated Slave**
S9-2	ON	OFF	OFF
S9-3	OFF	OFF	ON
S9-4	OFF	OFF	ON

5 BOARD LOGIC DESCRIPTION

The FPGA provides the foundation that allows Port 0 and Port 1 to work simultaneously or independently in Point-to-point, Switched Fabric and Arbitrated Loop topologies. The structure of each port supports the operating scenarios for simulating, generating, analyzing and corrupting the Fibre Channel data streams. As shown in Figures 5-1 and 5-2 and discussed in the following sections, the main components providing the board functionality are as follows:

- IRIG Decoding/Generating
- PCI/PCI-X Interface
- FPGA Port Logic
- PowerPC
- SERDES Interface
- Analyzer
- Generator
- Media Access Controller (MAC)

5.1 IRIG Encoding/Decoding

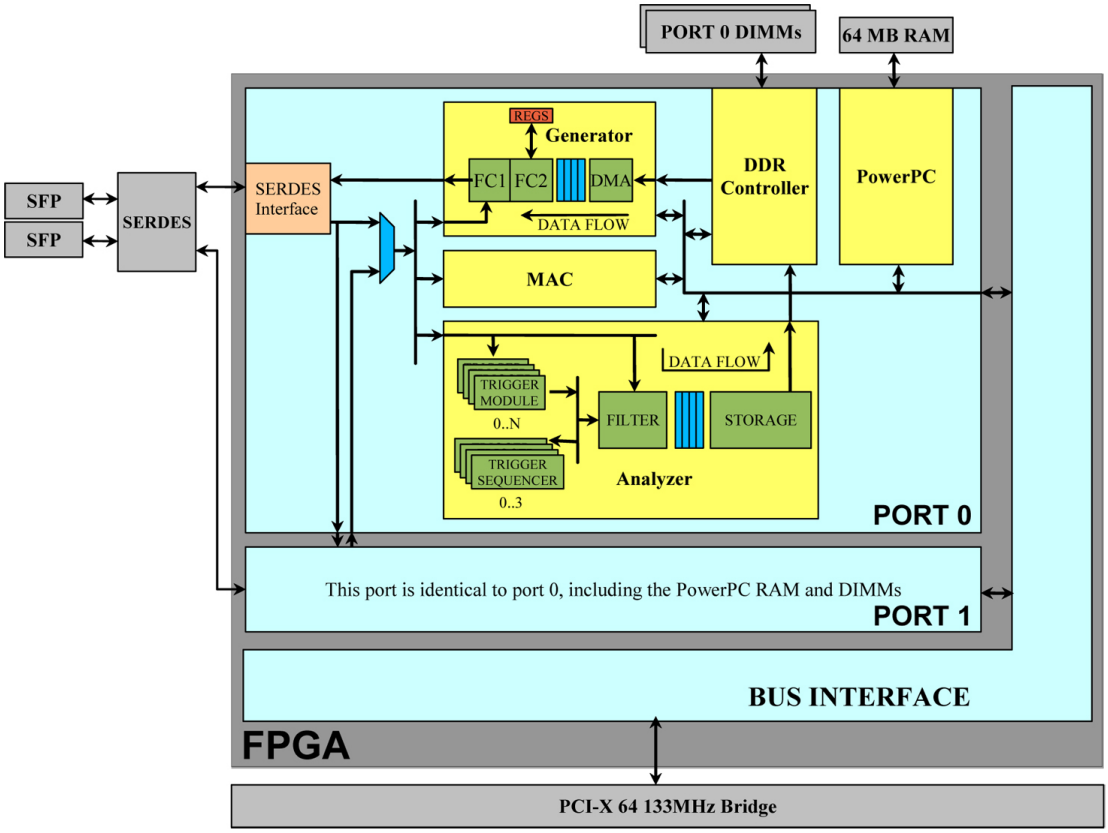
The FPGA internal clock decodes and generates the IRIG for applications requiring time stamping and re-clocking the data. The IRIG decoder provides time synchronization with an external IRIG source. The IRIG generator provides a synchronization source for multiple boards in a system. When used without an external IRIG source, the user can initialize the internal clock using a host clock or manually entering a start time. Once initialized, the internal clock is independent of the host clock. The internal or external IRIG provides precision time stamping for all captured data in the monitor log.

NOTE: IRIG is implemented with time code B modulated carrier only. (IRIG-B122)

5.2 PCI/PCI-X Interface

The PCI Interface embedded in the FPGA provides Direct Memory Addressing (DMA) capability to the module. The DMA controls the transmit data to the module and stores the received data from the module. This is a standard 33 MHz, 64-bit PCI interface on the APGFC2. The APG-FC4 extends this capability to allow up to a 133 MHz PCI-X interface.

Figure 5.2-1 Board Logic Structure of the APG-FC4



5.3 Port Logic

The FPGA defined Fibre Channel ports are identical. Each port has a dedicated PowerPC processor and user configurable data storage DIMMs. The ports are structured with an analyzer, generator and Fibre Channel Media Access Controller (MAC) embedded in the firmware. Additional port logic exists to multiplex data between the ports, allowing them to work together or independently.

5.3.1 PowerPC

The Power PCs for each port execute user defined C/C++ programs, as well as large sections of the application interface. This allows the user complete flexibility for data dependant simulation and error injection. Standard application interface function calls are used to write customized program applications for the PowerPC. Please refer to the **Software Library Reference Manual** for detailed descriptions of the application interface function calls, header files and sample program descriptions.

5.3.2 SERDES Interface

The SERDES interface handles the 8B/10B encoding and decoding, as well as controlling the input multiplexing. Each port can be configured to feed the ports transmit or receive data, or the opposing port's transmit or receive data into the analyzer, MAC, and generator. The application interface exposes these multiplexer configurations as a variety of inline and point-to-point topologies for the user to select.

5.3.3 Analyzer

Each port's analyzer has the capability to capture and synchronize raw data, including errors, across multiple streams. All data, including headers and payload, may be accessed and become criteria for triggering and filtering. The functional components of the Analyzer include:

Trigger Modules - Trigger modules perform initial data qualification, finding various user-programmed and predefined events in the data stream. The trigger modules are programmable using application interface function calls to output trigger events on:

- Data patterns within frames
- Specific ordered sets or data words
- Elapsing time periods
- Error conditions
- Counted occurrences of any of the other trigger modules

Trigger Sequencers - Trigger sequencers feed off of the trigger modules,allowing complex multi-level triggering for analyzing data. The trigger sequencers allow multi-level conditional triggering logic for the system. Trigger sequencers can be programmed to control the start and stop of the timer and counter trigger modules. Using the output of the trigger modules, the sequencers generate the following four trigger events:

- Internal trigger to mark a specific event in the capture buffer
- FIFO sequencer tags a variety of frames and events for simulation control
- External trigger drives the external trigger output for a port
- A generator trigger gates generator events

Filter Module - The filter module also feeds off of the trigger modules, so users can filter out or only store programmed frames and ordered sets. The filter module sets a default policy that either stores or drops everything. Individual ordered sets and frame trigger modules can be set to match or invert this policy for a given event. This allows the user to store or filter the defined data.

Storage Options - The storage module captures data to the port's DIMMs. The data capture parameters define how much data to store before the trigger position and the allocation of the port RAM for the capture. The internal trigger sequencer controls the trigger position occurrence for this module.

5.3.4 Generator

Each port generator has the capability to generate or corrupt data on the output. The user is provided with the controls to generate random, incrementing, decrementing or custom defined data on the output, program frame sequence gaps, and perform timing and data disparity calculations. CRC generation, disparity calculation and fill word injection between frames are handled by the generator, but can be turned off on a frame-by-frame basis. User defined data can trigger error injection in the headers or payload.

The Generator uses the Media Access Controller (MAC) for flow control or can be programmed to transmit user defined data, including error injection and data corruption.

The functional components/capabilities of the Generator include:

- **DMA Chaining Controller** - The DMA controls the input of data into the generator. These controllers have four priority transmit channels. Each transmit channel data stream can be programmed for delays or pauses to wait for generator sequencer events allowing lower priority channels to transmit.
- **Payload Replacement** - The generator allows frame content to be modified during transmission. This enables single transmit frames to be sent continuously with new or defined data values (such as OX_ID or S_ID). These transmitted frames can be cached for subsequent frames. Incrementing and random data generators are available for replacing general purpose registers and payload information.

5.3.5 Media Access Controller (MAC)

The Media Access Controller (MAC) manages the flow control of the data buffers for the generator. The MAC tells the generator when data may be sent and what primitive to send in FC applications. When interfacing with off-the-shelf FC devices, the user's simulation code is not required to manage the BB_credit because the MAC manages the BB_credit. The functional capabilities of the MAC include:

- **Flow Control** - The generator works with the MAC to send frames based on the number of BB_Credits currently granted to the port.
- **N_Port/L_Port Initialization** - In coordination with the MAC, the generator can insert the proper N_Port/L_Port primitives into the transmit data stream to initialize the link in either N_Port or L_Port mode.

6 TECHNICAL DATA

Processors:	Dual PowerPC @ 318 MHz
Memory:	512 MB, 1 GB or 2 GB DIMMs/port (Monitor/Transmit buffer) 64 MB RAM/port (PowerPC Instruction/ Data RAM)
Time Tagging:	For absolute time tagging a special time code processor implements a 46 Bit time tag
Time Synchronization:	
IRIG input Resolution:	<10 ns
Width:	14 BCD digits (400 days)
Signal Type:	Single ended analog
Signal Waveform:	Amplitude modulated sine wave or square wave
Modulation Ratio:	3:1 to 6:1
Input Amplitude:	0.2Vp-p to +3Vp-p
Input Impedance:	>3k Ohm
Coupling:	AC coupled
Time Jitter:	+/- 5 ns (typical, module-to-module) depending on input signal quality
Lock time:	1 to 5 seconds depending on input signal quality
IRIG output Signal Type:	Single ended analog
Signal Waveform:	Amplitude modulated square wave
Modulation Ratio:	3:1
Output Amplitude:	+/- 1.5 Volts
Output Impedance:	1.3 ohms typical (designed for 50 ohm load)
Time Sync Inputs (APG-FC4 only) Signal Type:	Differential RS485 or RS422
Signal Waveform:	Square wave/NRZ
Frequency:	10 MHz It is recommended that this only be ised in conjunction with an external clock source that is synchronized with it. If not, the LSD may be reset at a time skewed to the clock source. This could result in missing times or non-monotonic operation.
Input Amplitude:	+/- 100 mv to +/- 5 volts
Input Impedance:	22 K ohms minimum

Time Sync Outputs (APG-FC4 only) Signal Type:	Differential RS485 or RS422
Signal Waveform:	Square wave/NRZ
Frequency:	10 MHz
Output Amplitude:	1.5 p-p 25 ohm load RS485 2 p-p 50 ohm load RS 422
Driver Type:	Linear Technology LT1688
Receiver Supply:	+/- 5 volts
Triggers:	
Trigger Inputs (APG-FC2) Signal Type:	CMOS
Input Amplitude:	2.5 to 5 volts (1.25 volt threshold)
Receiver Type:	Fairchild 74LCX541MTC
Receiver Supply:	2.5 volts (5 volt tolerant inputs)
Trigger Inputs (APG-FC4) Signal Type:	Differential RS485 or RS422 or CMOS
Input Amplitude:	+/- 100 mv to +/- 5 volts
Input Impedance:	22 K ohms minimum
Common-mode range:	-7 to 12 volts
Receiver Type:	Linear Technology LT1518
Receiver Supply:	+/- 5 volts
Trigger Outputs (APG-FC2) Signal Type:	CMOS
Output Amplitude:	0 to 2.5 volts no load
Output Impedance:	50 ohms
Driver Type:	Fairchild 74LCX541MTC
Receiver Supply:	2.5 volts
Trigger Outputs (APG-FC4) Signal Type:	Differential RS485 or RS422 or CMOS
Output Amplitude:	1.5 p-p 25 ohm load RS485 0 to 5 volts no load
Driver Type:	Linear Technology LT1688
Receiver Supply:	+/- 5 volts
Connectors: Front Panel:	Two SFP sockets accept AIT delivered fibre transceivers or wire (copper) High density 26 pin D-Sub for I/O IRIG and Trigger (APG-FC2) High density 26 pin D-Sub for Time-Sync, I/O IRIG, and Trigger (APG-FC4)
Internal:	Four pin 0.1 x 0.025" header for board-to-board Timer-Sync interconnection
PCI backplane:	64 bit PCI Rev. 2.2 compliant (APG-FC2) 64 bit PCI Rev. 2.3 compliant (APG-FC4) 64 bit PCI-X Addendum to the PCI Local

	Bus Specification, Revision 1.0a compliant (APG-FC4)
Dimensions:	Full PCI form factor 312 x 107 mm
Supply Voltage:	+5.0 Vdc and +12.0 Vdc
Power (Idle):	
Voltage:	+5.0 V to +12.0 V
APG-FC2:	18 W to 1 W
APG-FC4:	22 W to 1 W
Power (Operating):	
Voltage:	+5.0 V to +12.0 V
APG-FC2:	24 W to 1 W
APG-FC4:	36 W to 1 W
Temperature:	0 to +45° C Standard Operating -40 to +85° C Storage
Humidity:	5 to 95% (non-condensing)

7 NOTES

7.1 Abbreviations and Acronyms

ASM	Anonymous Subscriber Messaging
BB	Buffer-to-Buffer
BIP	Bus Interface Processor
BIU	Bus Interface Unit
CRC	Cyclical Redundancy Check
CVT	Current Value Table
DDR	Double Data Rate
DIMM	Dual Inline Memory Module
DMA	Direct Memory Addressing
DRAM	Dynamic Random Access Memory
EDO	Enhanced Data Output
FC1	Fibre Channel FC-1 Level
FC2	Fibre Channel FC-2 Level
FC4	Fibre Channel FC-4 Level
FLASH	Page-oriented electrical erasable and programmable Gate Array
FPGA	Field Programmable Gate Array
Gb	Gigabit
GB	Gigabyte
Gbps	Gigabits per second
GUI	Graphical User Interface
I/O	Input/Output
INPUT_N	Input Negative
INPUT_P	Input Positive
IRIG	Inter Range Instrumentations Group
LED	Light-emitting Diode
MAC	Media Access Controller
MIL-STD	Military Standard
MUX	Multiplex
OUT_N	Output Negative
OUT_P	Output Positive
PCI	Peripheral Component Interconnect
PPC	PowerPC
ppm	parts per million
RAM	Random Access Memory
RISC	Reduced Instruction Set Computer
SDK	AIT Software Development Kit
SDRAM	Synchronous Dynamic Random Access

	Memory
SFP	Small Form Factor Pluggable
SRAM	Static Random Access Memory
Vdd	Voltage to drain